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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,185	09/24/2002	Johni Chan	73543	6299

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,185	CHAN, JOHNI	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/27/2006 amendment*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-31* is/are pending in the application.

4a) Of the above claim(s) *31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 23-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Pincus et al. (Pincus).

With regard to claim 23, Pincus discloses a redundant bus controller (RBC) for controlling access to a bus (multiple CPU registers provided in CPU register array 88 define the redundant bus controllers) , comprising: a peer coupling to communicate state information of the RBC to another bus controller for coordinating control of a bus between a plurality of system hosts (it is clear from Pincus that each CPU 40, for example, are coupled to another CPU 40 shown in Figs. 5 and 7, and coupled to the at least multiple registers provided by register arrays 88 shown in Fig. 7 to communicate state information); a control and status register configured to retain the state information of the RBS (it is clear that in Pincus, multiple CPU registers are provided in CPU register array 88, including the CPU barrier control and status register (suitably one per node, with one bit per CPU) which may be used to indicate and determine when a CPU

is at a barrier state, a hold mask enable control and status register which allows individual or multiple CPUs on a node to be placed in a "HOLD" condition (i.e. suspended from using the node bus) when both a hold mask enable bit and a CPU barrier bit for the corresponding CPU are set, and a configuration mask control and status register which allows software to configure CPUs into or out of the node. Each CPU is represented by a bit in the configuration mask control and status register whereby the currently available CPUS in the configuration register can define the "next" CPU. The node arbitration control and status register contains the value associated with the CPU on the node having highest round robin priority within a node. A software interrupt control and status register (also included in array 88) allows individual or multiple CPUS to be interrupted by a write to the register (or returns status when read). The CPU registers may be accessed locally by the processing elements on the node without any access to the memory system), and a sequencer configured to transition the RBC between a state in which the RBC is connected to the bus and a state in which the RBC is disconnected from the bus according to the state information retained in the control and status register (in Pincus, multiple CPU registers provided in CPU register array 88 define the redundant bus controllers. The RBC comprises a sequencer 24 having an array of CPU registers included in multiple registers provided by register arrays 88 that are manipulated by the processing elements on the bus based on whether they are requesting, using or releasing data bus 16. Each processor reads the CPU registers in sequencer 24 prior to accessing memory 14 to determine if the processor is allowed access. When access to the bus is given, the processor transfers

data to memory 14 and then disables a register bit in a register of sequencer 24. Sequencer 24 then enables the processor with the next highest priority to transition the state of the apparatus. Further, in Pincus, multiple CPU registers are provided in CPU register array 88, including the CPU barrier control and status register (suitably one per node, with one bit per CPU) which may be used to indicate and determine when a CPU is at a barrier state, a hold mask enable control and status register which allows individual or multiple CPUs on a node to be placed in a "HOLD" condition (i.e. suspended from using the node bus) when both a hold mask enable bit and a CPU barrier bit for the corresponding CPU are set, and a configuration mask control and status register which allows software to configure CPUs into or out of the node. Each CPU is represented by a bit in the configuration mask control and status register whereby the currently available CPUS in the configuration register can define the "next" CPU. The node arbitration control and status register contains the value associated with the CPU on the node having highest round robin priority within a node. Thus, it is clear that in Pincus, The RBC comprising a sequencer 24 having an array of CPU registers included in multiple registers provided by register arrays 88, is configured to transition the RBC between a state in which the RBC is connected to a bus and a state in which the RBC is disconnected to the bus).

With regard to claims 24 and 25, in Pincus, either the node arbitration control and status register (provided by register array 88 and connected to arbiter 52/144) or the arbitration control register 300 is readable as a register interface coupled to an arbiter. The node arbitration control and status register contains the value associated with the

CPU on the node having highest round robin priority within a node. See also Figs. 12(a, b) and description thereof.

With regard to newly added claim 26, either the node arbitration control and status register (provided by register array 88 and connected to arbiter 52/144) or the arbitration control register 300 is readable as a register interface. It is clear that a software access can be provided to the register interface via the node's external bus. In particular, in Pincus, multiple CPU registers are provided in CPU register array 88, including the CPU barrier control and status register (suitably one per node, with one bit per CPU) which may be used to indicate and determine when a CPU is at a barrier state (hereinafter described), a hold mask enable control and status register which allows individual or multiple CPUs on a node to be placed in a "HOLD" condition (i.e. suspended from using the node bus) when both a hold mask enable bit and a CPU barrier bit for the corresponding CPU are set, and a configuration mask control and status register which allows software to configure CPUs into or out of the node. Each CPU is represented by a bit in the configuration mask control and status register whereby the currently available CPUs in the configuration register can define the "next" CPU. The node arbitration control and status register contains the value associated with the CPU on the node having highest round robin priority within a node. A software interrupt control and status register (also included in array 88) allows individual or multiple CPUs to be interrupted by a write to the register (or returns status when read). The CPU registers may be accessed locally by the processing elements on the node without any access to the memory system. It is also clear tha setting arbitration logic for

arbitration control register 300 is performed using software. Setting the arbitration bit in arbitration control register 300 sets the highest priority node to `0`. When a memory port request is present, the highest priority processor node requesting access to a given memory port is allowed the current cycle for memory access. Once a node wins arbitration, the PAL encodes the P(7:0)M7ACK signals indicating which node has won. At completion of the arbitration cycle the current requester is placed at the bottom of the priority level and the next numerical requester becomes the highest priority. For example, when processor node P1 and processor node P3 are the first requesters after a system reset or a software set, processor node P1 has the highest priority level, making P3 the next highest level requester. Processor node P1 is given access to the memory port and at the completion of the arbitration cycle, node P1 is placed at lowest priority, making node P2 the highest level requester. If processor node P2 is not presenting a request for the memory port then node P3 is passed priority and transfers data during the next arbitration cycle. At the completion of the data transfer from processor node P3 to the memory port, processor node P3 is placed at the bottom of the priority level making processor node P1 the highest priority requester.

With regard to claim 27, the configuration register defines the next CPU to receive control, when synchronizing CPUs and nodes. For example, if the configuration register shows CPUs 1, 3, 4 and 7 as being configured, and CPU 1 is presently operating, the next CPU is 3, followed by 4, followed by 7. If CPU 7 is presently transferring data, once CPU 7 completes the data transfer, control of the node bus is given to CPU 1. The sequential ordering above is

given by way of example and is not intended as a requirement. The hold mask enable register, CPU barrier register, node barrier register, and the configuration register are used in conjunction with each other to reduce bus conflicts, synchronize processing elements within each processing node and between processing nodes, and to effectively process non-parallel applications.

With regard to claim 28, it is clear that in Pincus, the memory or I/O devices is readable as a peripheral device controlled by a host.

With regard to claim 29, see discussion above.

With regard to claim 30, multiple CPU registers provided in CPU register array 88 define the redundant bus controllers connected to a plurality of hosts. It is clear that even one host fails the multiple CPU registers provided in CPU register array 88 are still configured to coordinate control of the bus.

Response to Arguments

Applicants' arguments filed 2/27/2006 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is

the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The Pincus Rejection:

Applicants argue that "Pincus et al. describes wherein individual register bits within the sequencer 24/CPU register array 88 can be enabled and disabled (see Pincus et al. column 9, lines 39-45; column 13, line 30 to column 15, line 11) but fails to teach wherein the sequencer 24 is configured to transition the RBC (i.e., the CPU register 88 – see page 2 of Office Action mailed October 26, 2005) between a state in which the RBC is connected to a bus and a state in which the RBC is disconnected to the bus, as now recited in claim 23. To the contrary, the RBC of Pincus et al. must always be connected to the data bus 66 so that it can communicate with processor elements 40. Therefore, the sequencer 24 of Pincus et al. cannot be configured to transition the RBC therein between a state in which the RBC is connected to a bus and a state in which the RBC is disconnected to the bus, as the claim 23 recites."

In response to Applicants' argument, at the outset, it is noted that as clearly explained in the rejection set forth above, multiple CPU registers provided in CPU

register array 88 define the redundant bus controllers. The RBC comprises a sequencer 24 having an array of CPU registers included in multiple registers provided by register arrays 88 that are manipulated by the processing elements on the bus based on whether they are requesting, using or releasing data bus 16. Each processor reads the CPU registers in sequencer 24 prior to accessing memory 14 to determine if the processor is allowed access. When access to the bus is given, the processor transfers data to memory 14 and then disables a register bit in a register of sequencer 24. Sequencer 24 then enables the processor with the next highest priority to transition the state of the apparatus. As also explained the rejection set forth above, in Pincus, multiple CPU registers are provided in CPU register array 88, including the CPU barrier control and status register (suitably one per node, with one bit per CPU) which may be used to indicate and determine when a CPU is at a barrier state, a hold mask enable control and status register which allows individual or multiple CPUs on a node to be placed in a "HOLD" condition (i.e. suspended from using the node bus) when both a hold mask enable bit and a CPU barrier bit for the corresponding CPU are set, and a configuration mask control and status register which allows software to configure CPUs into or out of the node. Each CPU is represented by a bit in the configuration mask control and status register whereby the currently available CPUS in the configuration register can define the "next" CPU. The node arbitration control and status register contains the value associated with the CPU on the node having highest round robin priority within a node. Thus, it is clear that in Pincus, The RBC comprising a sequencer 24 having an array of CPU registers included in multiple registers provided by register

arrays 88, is configured to transition the RBC between a state in which the RBC is connected to a bus and a state in which the RBC is disconnected to the bus.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 571-272-3626.

Khanh Dang
Primary Examiner